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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PAI-HUNG PAN

Appeal 2008-1099
Application 09/944,506
Technology Center 2800

Decided: August 12, 2008

Before EDWARD C. KIMLIN, CHUNG K. PAK, and
THOMAS A. WALTZ, *Administrative Patent Judges*.

WALTZ, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant seeks review under 35 U.S.C. § 134 from the Examiner's rejections of pending claims 1-4, 6, 13, 18-19, 21, and 23-24 in the final Office Action.[1] This Board has jurisdiction under 35 U.S.C. § 6(b).

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[1] In the final Office Action dated Apr. 28, 2006, claims 7 and 9-12 were allowed and claims 5, 14, 20, and 22 were objected to as a matter of form. Claims 8 and 15-17 had been previously cancelled.

The invention in the present application relates to a precursor to a semiconductor device involving the formation of a shallow trench isolation structure. Independent claim 1 is exemplary and is set forth below.

> 1. A precursor to a semiconductor device structure, comprising:
>
> a semiconductor device layered structure comprising a semiconductor substrate;
>
> a buffer film layer located over at least a portion of the semiconductor substrate;
>
> at least one trench formed in the semiconductor device layered structure; and
>
> at least one shallow trench isolation structure positioned at least partially within the at least one trench and including:
>
> a substantially flat surface; and
>
> an integral ledge which extends laterally outward from the at least one trench, with no discernable boundary between the integral ledge and a remainder of the at least one shallow trench isolation structure, so as to contact only an area of an active surface of the semiconductor substrate adjacent the at least one trench.

The Examiner relies on the following prior art as evidence of unpatentability.

Morita	5,506,168	Apr. 9, 1996
Mandelman	5,521,422	May 28, 1996

The following rejections have been presented for review in this appeal:

Claims 1-4, 6, 13, 18, 19, 21, 23, and 24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Morita (Ans. 3).

Claims 1-4, 6, 13, 18, 19, 21, 23, and 24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Mandelman (*id.*).

ISSUES

1. Has Appellant shown the Examiner reversibly erred in finding the claims under review anticipated by either Morita or Mandelman?

FINDINGS OF FACT ("FF")

1. Appellant describes an embodiment of his invention in Fig. 10 of his drawings. The shallow trench isolation structure (126) comprises a ledge (130) which extends laterally outward from the remainder of the shallow trench isolation structure and contacts the adjacent semiconductor substrates surface (132). (Spec. 7).
2. The Specification describes the fabrication of a shallow trench isolation structure as first forming a layered structure (100) consisting of a semiconductor substrate (102), a dielectric layer (104), preferably silicon dioxide, and a buffer film layer (106). (Spec. 6*; See* Fig. 1).
3. The Specification describes the next fabrication step as etching a recess and subsequently a shallow trench in the layered structure. (Spec. 6; *See* Figs. 3 and 4).
4. The Specification describes the next fabrication step as lining the shallow trench with a thin layer of oxide (120). (Spec. 6*; See* Fig. 5).

5. The Specification describes the next fabrication step as etching back the buffer film away from the shallow trench. (Spec. 7*; See* Fig. 6).
6. The Specification describes the next fabrication step as filling the shallow trench with isolation material (122), which preferably is silicon dioxide. (*See* Fig. 7). In Fig. 7, the dielectric layer (104) and the oxide layer (120) are still present between the isolation material and the semiconductor substrate (102). The dielectric material is present between the isolation material (122) and the surface of the substrate, while the oxide is present between the trench walls and the isolation material (122).
7. The Specification describes the next fabrication step as removing the isolation material down to the buffer film layer (106). (Spec., p. 7*; see* Fig. 8). However, we find that Fig. 8, as well as Figs. 9 and 10, no longer displays separate layers of dielectric layer, oxide layer and isolation material, but rather one homogeneous isolation material 122. The Specification does not describe the removal, absorption, mixing or any other process by which the dielectric and oxide layers would no longer be present as shown in Fig. 7. (Spec., in its entirety).
8. Appellant describes the next fabrication step of his invention as removal of the buffer film layer. The remaining structure is referenced as an isolation structure (124). (Spec. 7*; see* Fig. 9). Finally, the isolation structure is etched to expose the substrate surface by removing the isolation structure (124) beyond the

ledge section. The remaining structure is referred to as the shallow trench isolation structure (126). (Spec. 7*; see* Fig. 10).

9. Morita describes a semiconductor substrate (1), a silicon nitride buffer film (30) and a shallow trench isolation structure comprising an element (3(37)) and the portion of layer (11) under (3(37)). (Ans. 3, *see* Morita, Fig. 72). The trench isolation structure includes a flat surface and an integral ledge extending outwardly from the trench and contacting only an area of an active surface of the substrate adjacent to the trench. (*Id).*
10. Mandelman discloses a trench isolation structure (32) comprising an insulator (18a) and an oxide layer (34) having an integral ledge (22c) in contact with the adjacent surface of the semiconductor substrate (10). (Ans.3-4, *see* Mandelman, Figs. 4a and 4b).

PRINCIPLES OF LAW

Under 35 U.S.C. § 102(b), a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently, described in a single prior art reference. *Verdegall Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631 (Fed. Cir. 1987).

Claims are given the broadest reasonable construction consistent with the specification. *In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997). The Patent and Trademark Office ("PTO") determines the scope of claims in patent applications not solely on the basis of the claim language, but upon

giving claims their broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re American Academy of Science Tech Center*, 367 F.3d 1359, 1364 (Fed. Cir. 2004). However, the broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. *In re Cortright*, 165 F.3d 1353, 1358, (Fed. Cir. 1999).

To properly compare a prior art reference with the claims at issue, the claim must first be correctly construed to define the scope and meaning of each contested limitation. *Gechter v. Davidson*, 116 F.3d 1454, 1457 (Fed. Cir. 1997). The specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005). Although claims are to be interpreted in light of the specification, limitations from the specification are not to be read into the claims. *See In re Van Geuns,* 988 F.2d 1181, 1184 (Fed. Cir. 1993). The scope of a disputed term is not limited by the preferred embodiments absent an express disclaimer by Appellant of a broader definition. *See In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004).

DISCUSSION

Claim construction

"Shallow Trench Isolation Structure"

At least two, and possibly all four, of Appellant's arguments for differentiating his claimed invention from the two prior art references turn

on the construction of the term "shallow trench isolation structure" recited in claim 1. Claim 1 does not explicitly define the shallow trench isolation structure nor is there an explicit definition of this phrase in the Specification. Appellant explicitly contends that the equivalent shallow trench isolation structure in both prior art references does not contact an area of the semiconductor substrate adjacent to the trench. (App. Br. 10).[2] In differentiating the invention from Morita, Appellant argues that, in Morita, the equivalent shallow trench isolation structure (3(37)), made from a silicon nitride film (37), is separated from the semiconductor substrate by a silicon dioxide film (11). Appellant contends that the shallow trench isolation structure (3(37)) therefore does not include the silicon dioxide film (11), as the two are formed separately and are of different materials. (*Id).*

In Appellant's disclosure, a homogeneous shallow trench isolation structure (126), as shown in Fig. 10, contacts the surface of the adjacent semiconductor substrate (102). However, this drawing appears misleading, as Appellant's shallow trench isolation structure was initially prepared, as shown in Fig. 6, by disposing an oxide film (120) on the interior surface of the trench, and a dioxide layer, called a dielectric layer (104), on the semiconductor substrate (102). Subsequently, an isolation material (122) is deposited over the entire structure (*see* Fig. 7). According to the Specification, the material of construction of both the dielectric layer (104) and the isolation material (122) is silicon dioxide (FF 1, 6). However, these are preferred materials, and the Specification does not limit these elements to only silicon dioxide. (Spec. in its entirety). However, Fig. 7 of the Specification shows distinct boundaries between the oxide layer 120 (FF 7),

[2] We refer to and cite from the Appeal Brief dated November 16, 2006.

the dielectric layer 104, and the isolation material (122) (FF 6), all of which are formed separately and not necessarily of the same material. Subsequently, Fig. 8 no longer shows any reference to or the boundary for the oxide layer (120). (FF 7). The Specification does not describe any removal or destruction of the oxide layer (120). Similarly, the dielectric layer (104) is referenced in Fig. 8, but no boundary, as had been shown in Fig. 7, is shown between it and the isolating material (122). Subsequently, in Figs. 9 and 10, all the prior references and boundaries are removed, and the composite structure of the oxide layer (120), the dielectric layer (104), and the isolation material (122) is now referenced as an "isolation structure." (Spec. 7). Subsequent to an etching of the buffer film layer (106), the structure is then referenced in Fig. 10 as the shallow trench isolation structure (126). (FF 8).

Therefore, we find that one of ordinary skill in the art in light of the teachings in the Specification would construe the term "shallow trench isolation structure" to mean the composite structure of the oxide film, the dielectric film over the substrate, and the isolating material, after subsequent etching to remove excess buffer film layer, regardless of the order of fabrication or materials of construction.

"No discernable boundary between"

In some of his arguments, Appellant raises an issue of whether the prior art exhibits "no discernable boundary between" the integral ledge and a remainder of the at least one shallow trench isolation structure. (App. Br. 10). As shown in Fig. 10 of the Specification, a ledge is referenced as (130), which is part of the shallow trench isolation structure (126) but is above and

extends laterally outward beyond the trench corner (128). Neither the claims nor the Specification describe or define any "discernable boundary," or lack thereof, between the integral ledge and the remainder of the shallow trench isolation structure. Only the drawings accompanying the Specification provide insight as to the meaning of this term.

As discussed *supra*, the term "shallow trench isolation structure," as shown in Fig. 10 of the Specification as reference (126), was fabricated from an oxide layer 120, a dielectric layer (104) and an isolation material (122), as shown in Fig. 7. As also shown in Fig. 7, a boundary is evident between the dielectric layer and the isolation material (122), with this boundary lying in a plane parallel to the surface of the semiconductor substrate. There is also another boundary evident in Fig. 7, between the interior edge of the dielectric layer (104) and the top exterior edge of the oxide layer (120). This second boundary is normal to the plane of the semiconductor substrate surface 102, and coplanar with the edge of the shallow trench. However, this boundary extends only as high as the thickness of the dielectric layer, and does not extend upward into the isolation material above the dielectric layer. While these boundaries are evident in Fig. 7, they are not in Figs 8-10, though the Specification does not describe any process in which the dielectric layer or the oxide layer, evident in Fig. 7, had been removed or mixed into the isolation material (122). As evident from Fig. 7, the term "no discernable boundary between" does not refer to any boundary between composite layers in the shallow trench isolation material parallel to the semiconductor substrate surface. Therefore, since we construe the term, "shallow trench isolation structure," *supra*, as a composite of several layers, we also construe the term "no discernable boundary between" as not

including a boundary between the composite structure and another structure, and not reading on any boundaries of the layers per se comprising the construction or formation of the shallow trench isolation structure.

"Only an area of an active surface of the semiconductor substrate adjacent the at least one trench."

In analyzing and construing the claims of an application, we must give the claim terms the broadest reasonable meaning in their ordinary usage as they would be understood by one of ordinary skill in the art, consistent with the specification. Nothing in Claim 1 or the Specification limits the width of the ledge structure, only that it is adjacent to the trench. The silicon dioxide layer, apparently being continuous, has no portion that is not adjacent to the trench. Alternatively, as the Examiner argues, nothing requires us to consider the entire silicon dioxide film, including that part extending beyond the ledge, as part of the isolation structure. This view is consistent with Appellant's Specification. In the Specification, an isolation structure (124) is first formed which, as shown in Fig. 9, extends beyond the ledge. The excess is etched during a subsequent wet oxide process, (Spec. 7), leaving the shallow trench isolation structure (126) depicted in Fig. 10. Thus, any excess of the former dioxide layer beyond the perimeter of the ledge need not be considered part of the shallow trench isolation structure.

35 U.S.C. § 102(b) – Anticipation by Morita

Claims 1-4, 6, 13, 18, 19, 21, 23 and 24 stand rejected under 35 U.S.C. § 102(b) as anticipated by Morita. Appellants direct their arguments collectively to independent claims 1, 13 and 18. App. Br. 11. Appellants do not argue separately for the patentability of the remaining dependent claims, *Id.,* but instead rely on the asserted patentability of the independent claims

upon which these remaining claims depend and inherit all limitations therein. Accordingly, we treat the claims as one group, to stand or fall together, with claim 1 as representative. 41 C.F.R. § 37(c)(1)(vii).

The Examiner contends that Morita teaches all the limitations of the claims (Ans. 3). Appellant traverses this rejection with three arguments. First, Appellant contends that, in Morita, the trench isolation structure (3(37)) does not directly contact the surface of the semiconductor substrate, a limitation of claim 1, but instead contacts a silicon dioxide film (11) between the trench isolation structure and the substrate surface. (App. Br. 10). This argument is premised on a construction that the trench isolation structure does not comprise a silicon dioxide film initially deposited on the substrate surface. However, as discussed *supra*, we have concluded that the proper construction of the term, "shallow trench isolation structure" includes any dielectric layer or silicon dioxide layer formed on the semiconductor substrate surface and later incorporated with the isolation material to form the ledge of a shallow trench isolation structure. Given our construction of the claim term, Appellant's argument is not persuasive.

Next, Appellant argues in the alternative that, if the silicon dioxide film (11) of Morita is part of the trench isolation structure, resulting in direct contact of the trench isolation structure with the semiconductor substrate surface, then "[t]his is in [direct] contradiction with the requirement … that an STI structure only contact portions of the active surface that are located 'adjacent the at least one trench.'" (App. Br. 10). Appellant does not argue, nor point to any part of the Specification, that may clarify any limit on the STI structure's dimensional limits beyond "adjacent". Only a preferred embodiment is provided. The Examiner responds that the portion of the

layer (11) in Morita not under the ledge is not part of the isolation structure. (Ans. 4). This is consistent with our construction of the claim phrase, "*only an area of an active surface of the semiconductor substrate adjacent the at least one trench*", *supra.*

Finally, Appellant argues that claim 1 requires at least one shallow trench isolation structure with no discernible boundary between an integral ledge and a remainder of the at least one shallow trench isolation structure, in contrast to the two films (11, 37) in Morita, which are fabricated at different times and of different materials, thereby resulting in a discernible boundary. However, consistent with our construction of the claim terms, this boundary between layers is not within the scope of the claim limitation. While not shown in Fig. 10, Appellant's Fig. 7 clearly shows a boundary between two layers formed at different times. This boundary is omitted from Fig. 10, but we have found no basis for believing it is not present as shown in Fig. 7. Further, while the two layers are each formed of the same material, they are only preferred embodiments. (*See* FF 2, 6). We are to avoid importing limitations from the Specification into the claims. *In re Van Geuns,* 988 F.2d at 1184. Thus, by our construction of this claim term, *supra*, the two layers in Morita do not exhibit a discernible boundary, within the meaning of that claim term. We therefore find, in accord with the above claim term construction, that Morita discloses, as a matter of fact, each of the limitations of the pending claims.

Accordingly, the Examiner's rejection of the pending claims is sustained.

35 U.S.C. § 102(b) – Anticipation by Mandelman

The Examiner further rejected the pending claims as anticipated by Mandelman. . Appellants direct their arguments collectively to independent claims 1, 13 and 18. App. Br. 11. Appellants do not argue separately for the patentability of the remaining dependent claims, *Id.,* but instead rely on the asserted patentability of the independent claims upon which these remaining claims depend and inherit all limitations therein. Accordingly, we treat the claims as one group, to stand or fall together , with claim 1 as representative. 41 C.F.R. § 37(c)(1)(vii).

The Examiner contends that Mandelman also discloses all limitations of the pending claims, Ans. 3-4, FF 10. Appellant traverses this rejection with two arguments. First, Appellant argues that a shallow trench isolation structure disclosed in Mandelman comprises a thermal oxide layer 34 separate from the STI structure, which Appellant identifies as Reference 18a, referred to in Mandelman as an insulator. (FF 10). Therefore, the shallow trench isolation structure, as construed by Appellant, does not contact the semiconductor substrate surface. As with the previous rejection, our construction of the claim term "shallow trench isolation structure" comprises any other layers in addition to the insulator, used in the formation of the shallow trench isolation structure, including any initial oxide coating of the shallow trench. Hence, by our construction of the claim term, Appellant's first argument is not persuasive.

Appellant then argues that, in Mandelman, the insulator 18a and the oxide layer 34 form a discernible boundary, contrary to the limitations of claim 1. (App. Br. 12). But, as in the rejection over Morita, we find Appellant's argument not persuasive by our construction of the claim term,

"no discernible boundary layer between," *supra*. We have concluded that boundary planes between layers comprising the shallow trench isolation structure parallel to the surface of the substrate surface are not within the scope of that claim limitation. In accord with our construction of the claim terms, we find, as a matter of fact, that Mandelman discloses all the elements of the pending claims.

Accordingly, the Examiner's rejection of the pending claims as anticipated by Mandelman is sustained.

CONCLUSION

The Appellant has failed to show the Examiner reversibly erred in finding the claims anticipated by either Morita or Mandelman. Accordingly, the rejections of the pending claims are sustained.

TIME PERIOD FOR RESPONSE

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

Appeal 2008-1099
Application 09/944,506

PL initial:
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